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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,198	12/08/2004	Jean-Paul Theis		3234

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/517,198	THEIS, JEAN-PAUL	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21
10/4/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 12/08/2004.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the four method steps (i.e. steps a-d) in claim 1 must be shown or the feature(s) canceled from the claim(s). The drawings show two steps of the method, whereas claim 1 claims four steps. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1-12 are objected to because of the following informalities: The phrases "in the following, said dedicated memory is referred to by the term heap address cache" and "said data are also called link data in the following;" in steps b and c, respectively, of claim 1 should be removed. Appropriate correction is required.

5. All claims objected to that have not been specifically addressed above are objected to on the basis of dependence.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lange et al., U.S. Patent No. 6,151,670 (Herein referred to as Lange).

8. Referring to claim 1, Lange has taught a method for implementing autonomous load/store within a data processing system by using symbolic machine code, where said

data processing system comprises a microprocessor and a memory system, where said memory system has a memory hierarchy containing: one or more register files of said microprocessor one or more data caches at different memory hierarchy levels a main memory where said microprocessor has an instruction set and where said instruction set contains one or more instructions of which one or more operands and/or results may specify one or more symbolic variables, where a symbolic machine code is running on said microprocessor, where said symbolic machine code contains one or more instructions of which one or more operands and/or results specify one or more symbolic variables, where said autonomous load/store refers to the loading and storing of data generated and used by said symbolic machine code and where at least part of said data loading and storing is done without requiring any explicit load/store instructions in said symbolic machine code, where each of said symbolic variables specifies one or more entries of a memory other than a register file of said microprocessor, where said entries are used by the microprocessor in order to determine the addresses within the memory hierarchy where the values of said symbolic variables may be stored to and/or loaded from during execution of said symbolic machine code *[column 2, lines 30-50]*, where said method comprises the following steps:

a. when the microprocessor fetches an instruction of which a result and/or one or more operands specify one or more symbolic variables, it computes the addresses within the memory hierarchy where the values of said symbolic variables may be stored into and/or loaded from *[the address of a short or long term register is computed based upon the register identifier; column 2, lines 51-62]*;

b. after anyone of said addresses has been computed, the microprocessor writes this computed address into an entry of a dedicated memory *[register addresses are written to memory with an indication of whether they are short or long term registers; column 3, lines 4-25]*;

c. in addition to said computed address of step b., said microprocessor writes data associated to said computed address into said heap address cache and/or into another memory; said link data are such that, when they are accessed by the microprocessor, they allow the microprocessor to make the link with or to associate them to said computed address and may be used to determine whether said computed address refers to the value of an operand and/or of a result of said instruction *[column 3, lines 4-25]*

d. the microprocessor uses said entry within said heap address cache in order to determine or estimate the lifetime *[term]* of the value to be stored to or to be loaded from said computed address *[column 2, lines 51-62]*

9. Referring to claim 2, Lange has taught a method as claimed in claim 1, where step d. is further specified as follows: the microprocessor uses said entry within said heap address cache and/or said link data in order to determine or estimate the lifetime of said value by determining or estimating the amount of time which elapsed since a previous write of the same address into an entry of said heap address cache *[column 2, lines 40-50]*;

10. Referring to claim 3, Lange has taught a method as claimed in claim 2, where said heap address cache is realized as a circular stack, where steps b. and c. are further specified as follows:

b. after anyone of said addresses has been computed, the microprocessor writes this computed address into the same entry of the circular stack as the one where the link data in step d. are written *[column 2, lines 51-62]*;

c. said microprocessor writes said link data into the same entry of the circular stack as said computed address, said link data comprising one or both of the following: a type-flag, which tells the microprocessor whether the value stored or to be stored at said computed address refers to the value of an instruction operand or of an instruction result a valid-flag, which tells the microprocessor whether the entry contains data which can be overwritten or not *[column 2, lines 51-62]*.

11. Referring to claim 4, Lange has taught a method as claimed in claim 3, where, in addition to the data mentioned in step c., said link data further contain an execution state value, this value allowing to determine the execution state of said symbolic machine code at the point in time when said instruction is fetched or when said link data are written *[column 3, lines 4-25]*.

12. Referring to claim 5, Lange has taught a method as claimed in claim 3, where step b. is further specified as follows: the microprocessor uses said entry within said heap address cache and/or said link data in order to determine or estimate the lifetime of said value by subtracting the entry containing said computed address from another entry of said heap address cache containing the same address *[column 2, lines 51-62]*;

13. Referring to claim 6, Lange has taught a method as claimed in claim 4, where step b. is further specified as follows: the microprocessor uses said entry within said heap address cache and said execution state value in order to determine or estimate the lifetime of said value by subtracting the execution state value stored in the entry containing said computed address from the execution state value stored in the same or in another entry of said heap address cache containing the same address *[column 2, lines 51-62]*;

14. Referring to claim 7, Lange has taught a method as claimed in claim 1, where the microprocessor uses the lifetimes of the values of said symbolic variables in order to determine the addresses and/or the hierarchy levels within the memory hierarchy where said values shall be stored *[column 2, lines 30-50]*;

15. Referring to claim 8, Lange has taught a method as claimed in claim 2, where the microprocessor uses the lifetimes of the values of said symbolic variables in order to determine the addresses and/or the hierarchy levels within the memory hierarchy where said values shall be stored *[column 2, lines 30-50]*;

16. Referring to claim 9, Lange has taught a method as claimed in claim 3, where the microprocessor uses the lifetimes of the values of said symbolic variables in order to determine the addresses and/or the hierarchy levels within the memory hierarchy where said values shall be stored *[column 2, lines 30-50]*;

17. Referring to claim 10, Lange has taught a method as claimed in claim 4, where the microprocessor uses the lifetimes of the values of said symbolic variables in order to

determine the addresses and/or the hierarchy levels within the memory hierarchy where said values shall be stored *[column 2, lines 30-50]*;

18. Referring to claim 11, Lange has taught a method as claimed in claim 5, where the microprocessor uses the lifetimes of the values of said symbolic variables in order to determine the addresses and/or the hierarchy levels within the memory hierarchy where said values shall be stored *[column 2, lines 30-50]* ;

19. Referring to claim 12, Lange has taught a method as claimed in claim 6, where the microprocessor uses the lifetimes of the values of said symbolic variables in order to determine the addresses and/or the hierarchy levels within the memory hierarchy where said values shall be stored *[column 2, lines 30-50]*;

20. Referring to claim 13, Lange has taught a microprocessor having an instruction set containing: one or more instructions of which one or more operands and/or results may specify one or more symbolic variables *[short or long term register identifiers]* one or more symbolic link instructions where said microprocessor is able to execute symbolic machine code *[instructions that include short or long term register identifiers]*, where said symbolic machine code contains one or more instructions of which one or more operands and/or results specify one or more symbolic variables *[column 2, lines 30-50]*.

Conclusion

21. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lozano et al., "Exploiting Short-Lived Variables in Superscalar Processors", teaches storing short-lived variables to memory outside of a processors register file.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
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